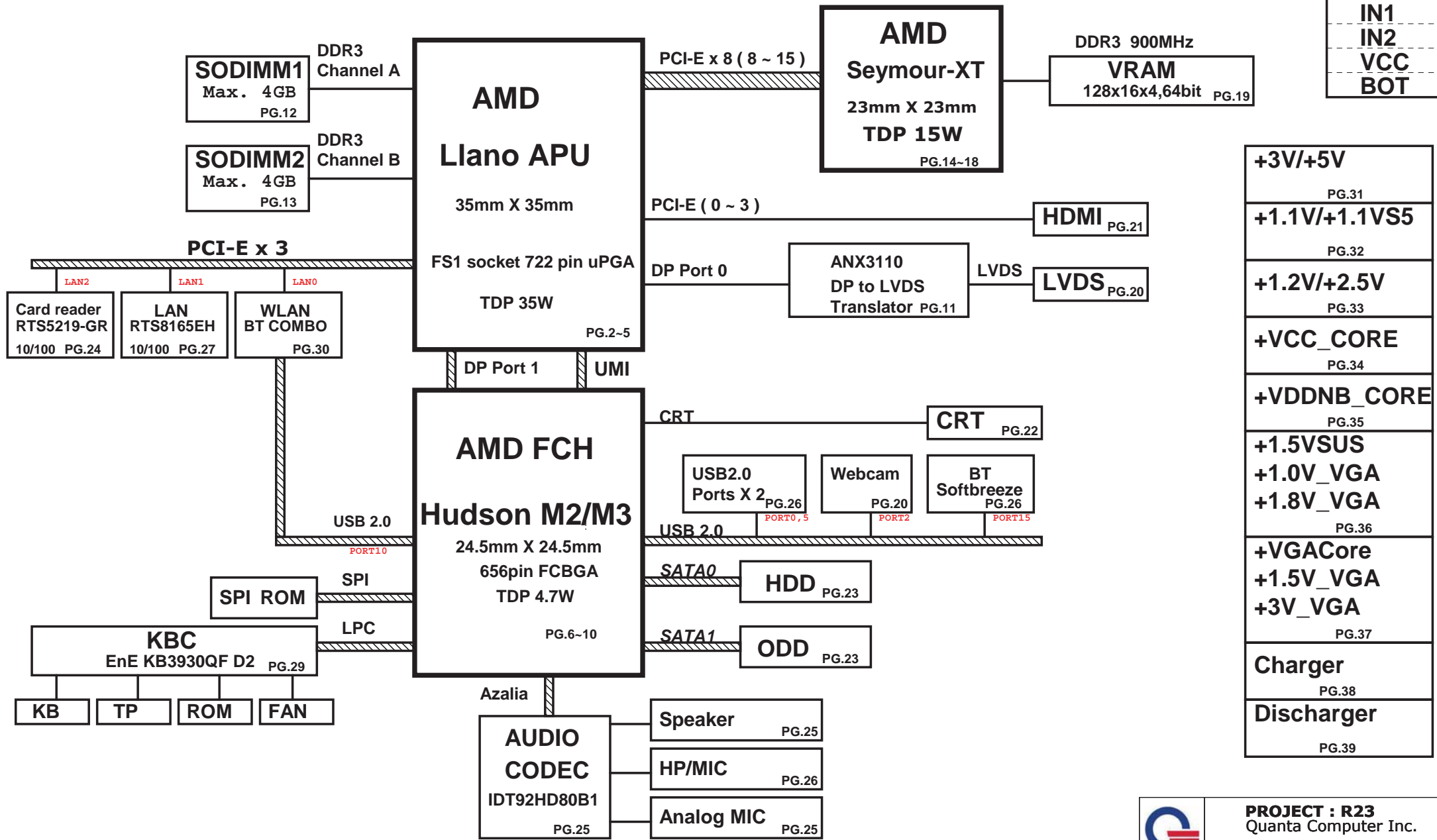


# R23 AMD Sabin UMI/Muxless SYSTEM DIAGRAM

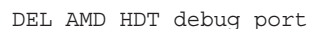
Stackup


TOP  
GND  
IN1  
IN2  
VCC  
BOT

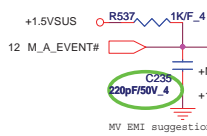
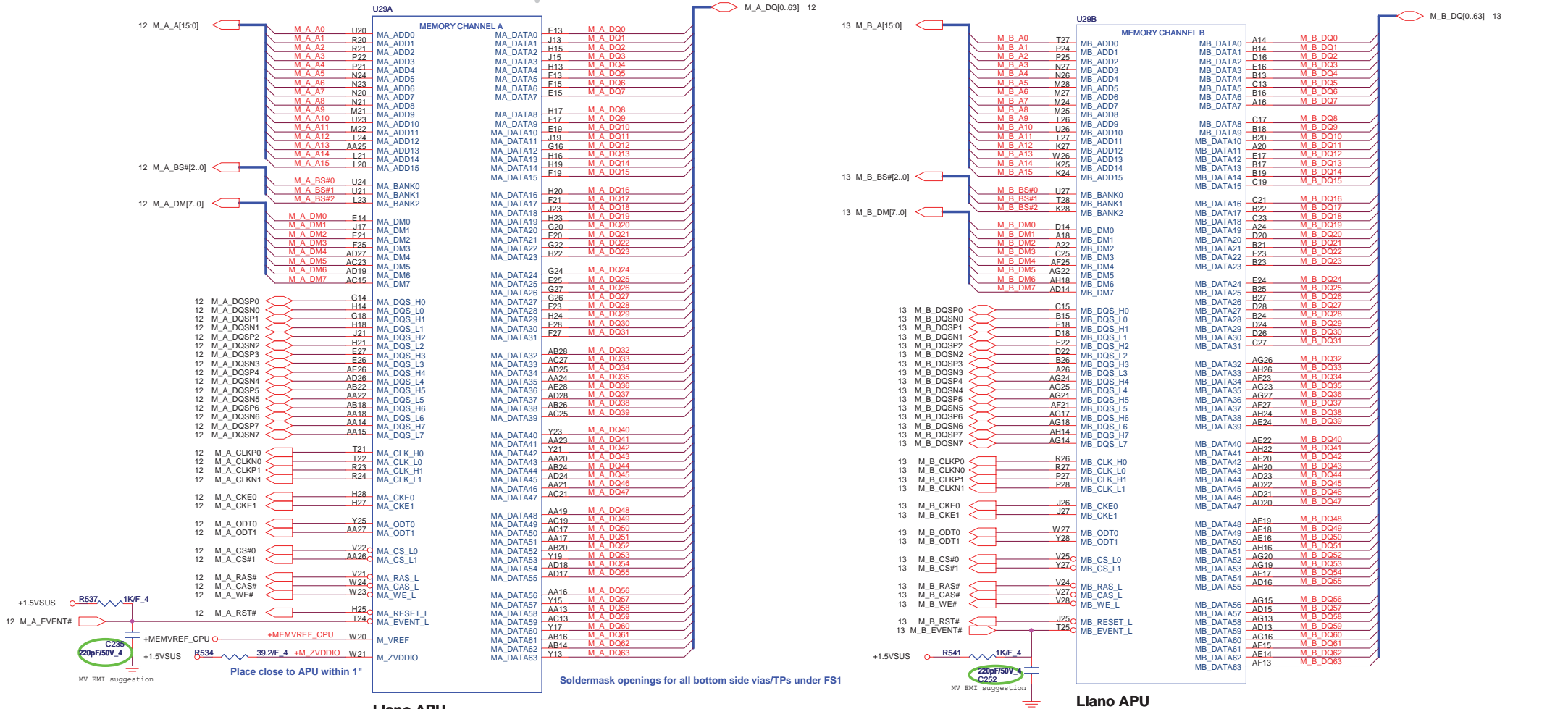




## VID Override Circuit



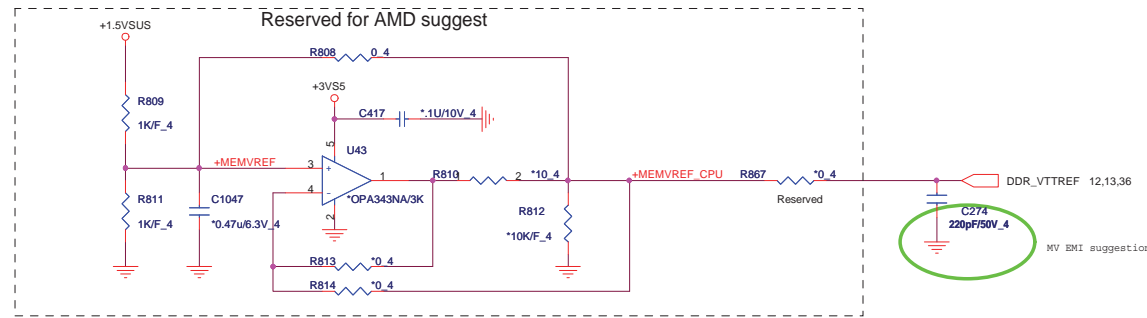
 <b>Quanta Computer Inc.</b> <b>PROJECT : R23</b>	
Size	Document Number <b>Liano PCIE/UMI/GPP</b>
Date: <b>Wednesday, May 04, 2011</b>	Sheet <b>2</b> of <b>40</b> Rev <b>1A</b>



Liano APU



Liano APU



DP0 output to  
eDP to LVDS converter

DP1 output to Hudson-M2  
for VGA translator interface

Note: CLK\_APU\_HCLKP/N is 100MHZ SSC

Note: CLK\_DP\_NSSCP/N is 100MHZ non-SSC

Display port power 1.5V min 1.2v max : 1.65v

Display port power 1.5V min 1.2v max : 1.65v

LVDS

VGA

HDMI

To AMD HDT

DMAACTIVE\_L controls  
entry and exit from the  
sleep and power states

AMD internal test only

FS1R1 signals is for detect CPU TYPE and protect it.  
FS1R1 CPU this pin is N.C  
FS1R2 CPU this pin is LOW  
can remove it at MP

Llano APU

APU\_PROCHOT# 可以當 input or output  
當Low時CPU會降 P- STATE

Thermal

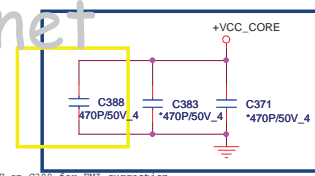
THERMTRIP# shutdown temperature 125度C

over 120 degree C= Low

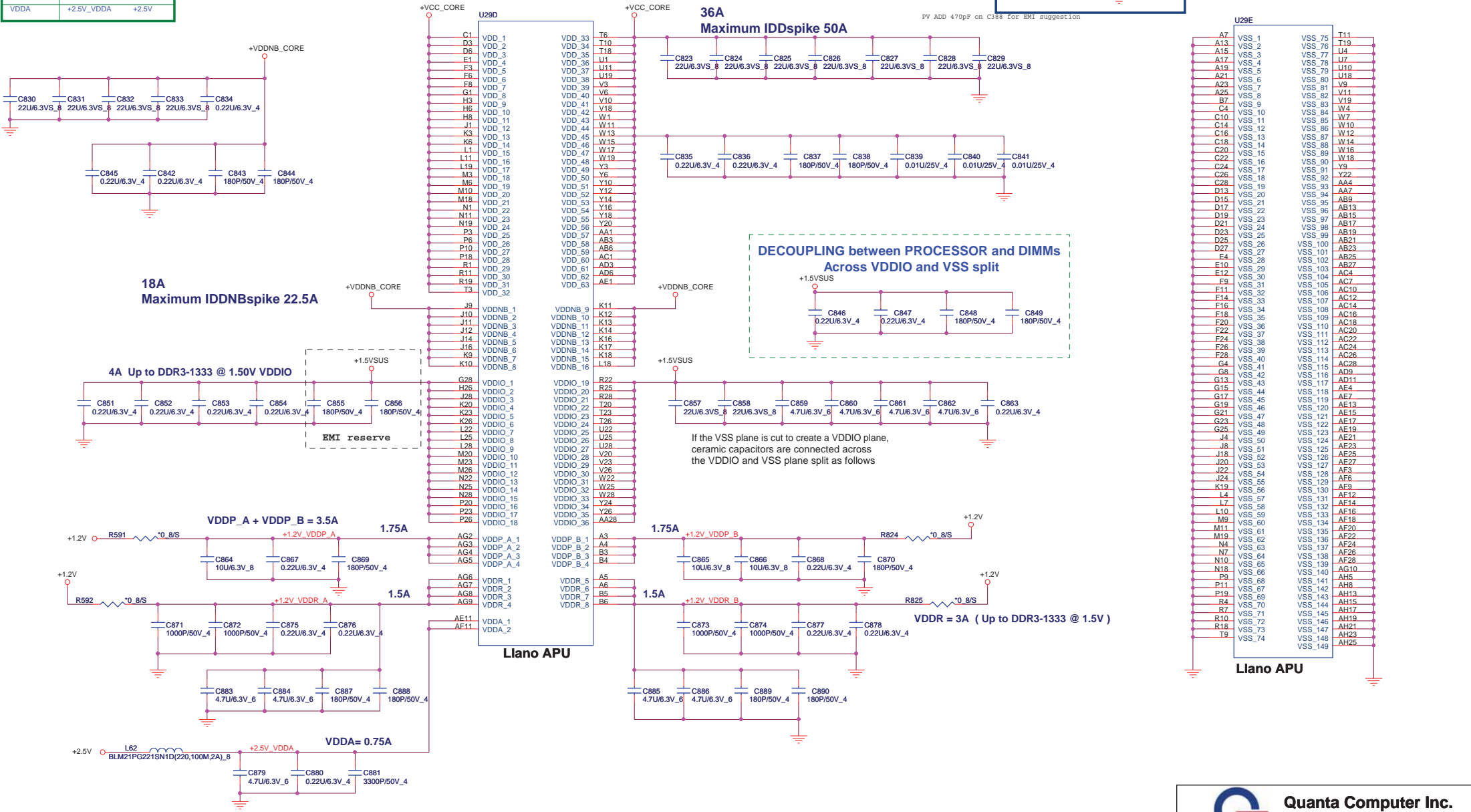
When 100K-NTC 100 C=6.164K  
Thermal Trip = 120 C


DEL Thermal IC circuit on MV

APU POWER TABLE		
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



SI EMI



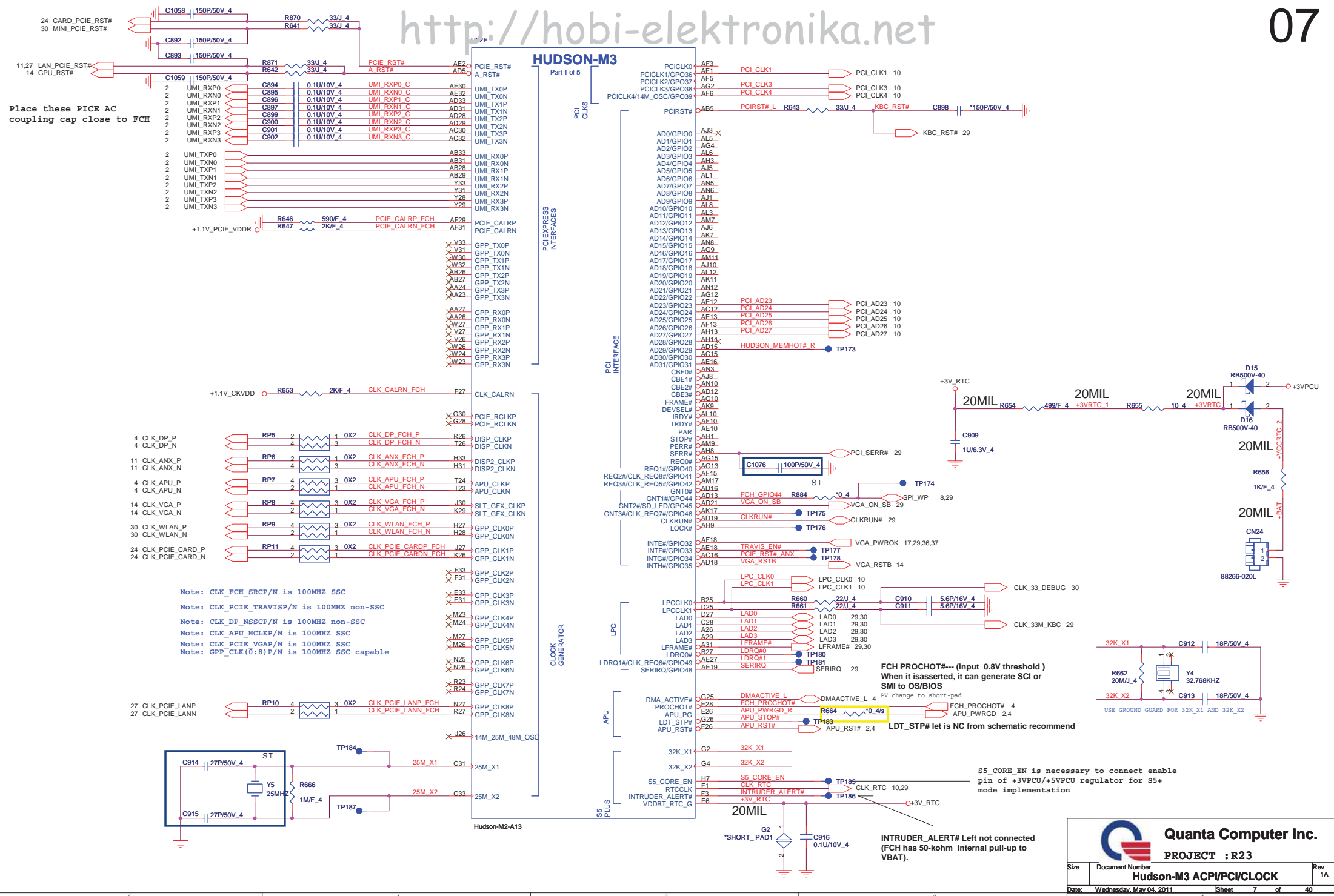


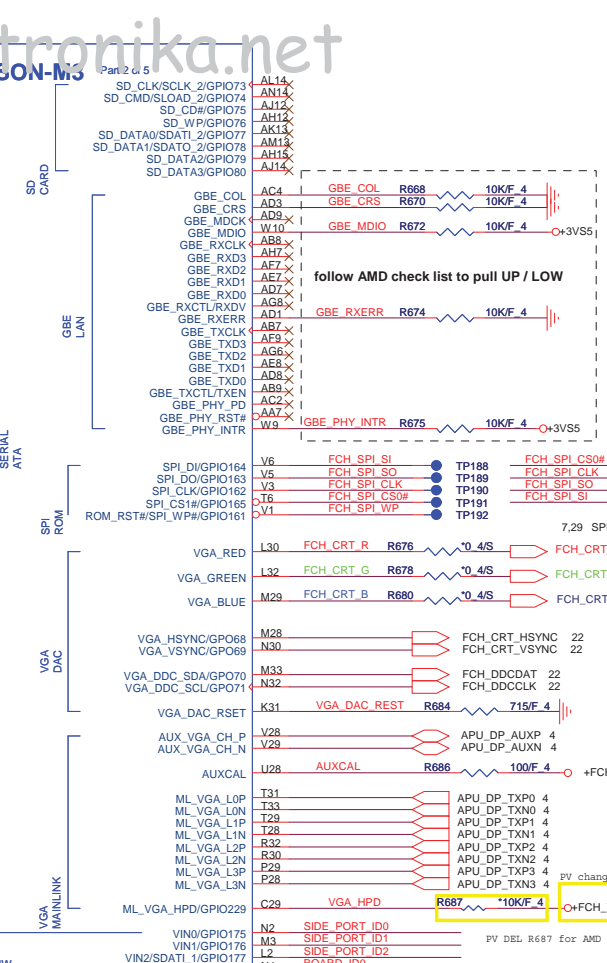
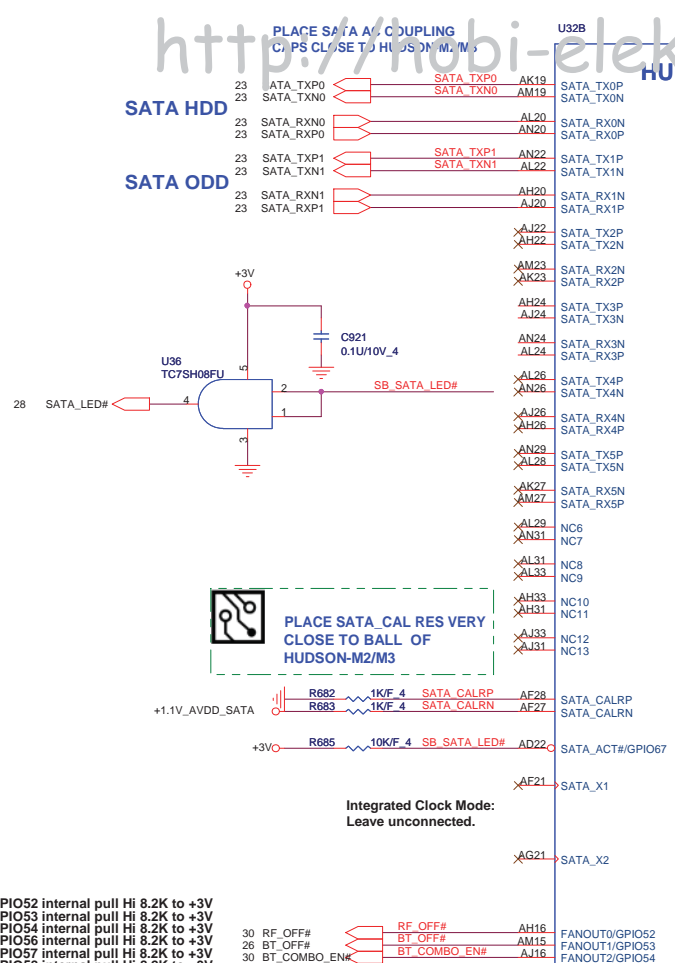
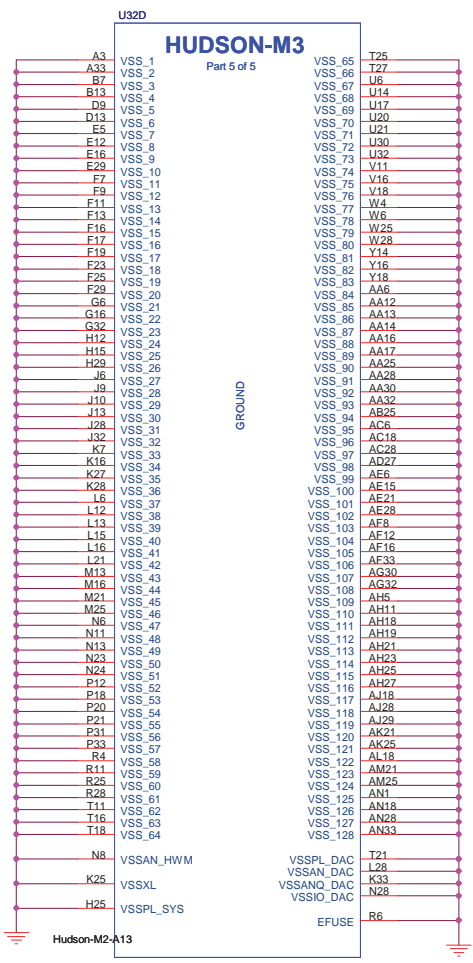
**Quanta Computer Inc.**  
**PROJECT : R23**

Size	Document Number	Llano POWER/GND	Rev. 1A
Date:	Wednesday, May 04, 2011	Sheet 5 of 40	

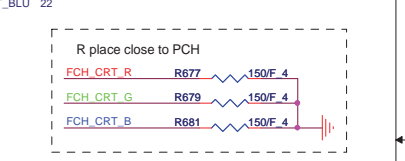
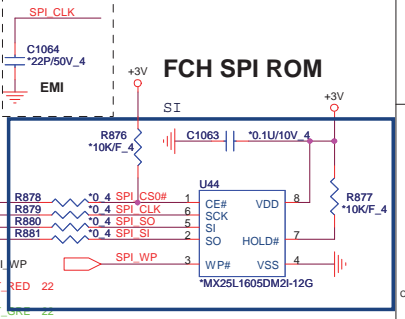




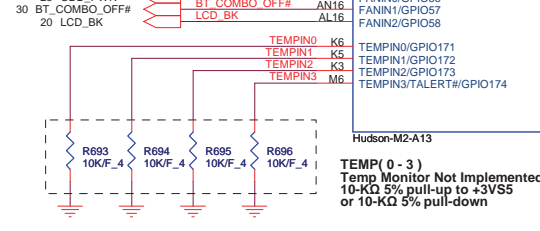




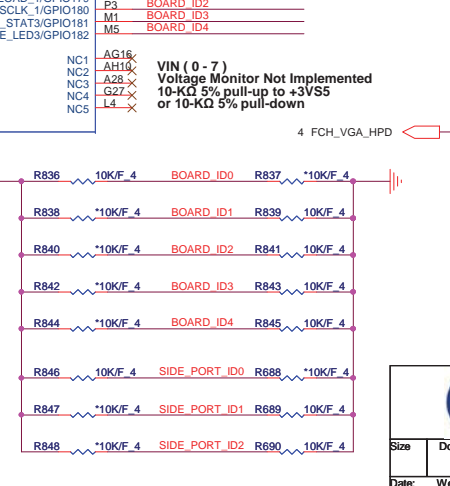
Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

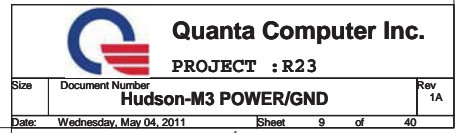


**Quanta Computer Inc.**  
PROJECT : R23

Size Document Number Hudson-M3 SATA/HWM/SPI Rev 1A

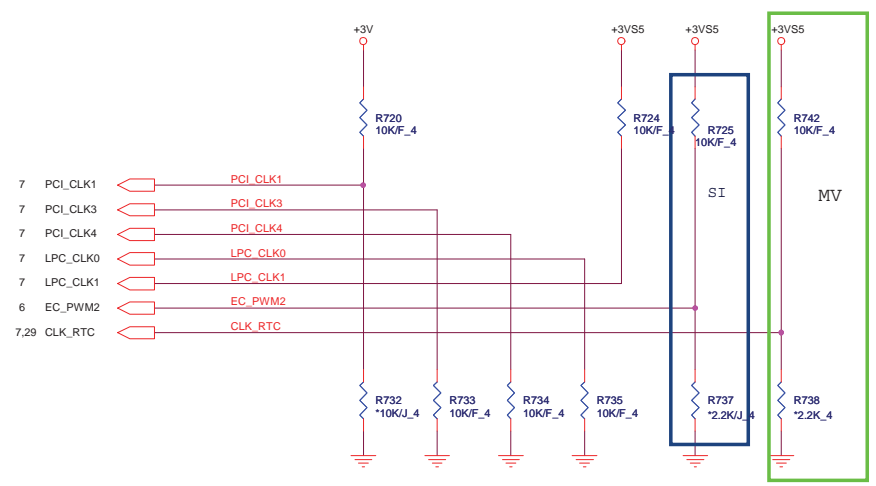
Date: Wednesday, May 04, 2011 Sheet 8 of 40





STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH		ALLOW PCIE Gen2 DEFAULT		USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW		FORCE PCIE Gen1		IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

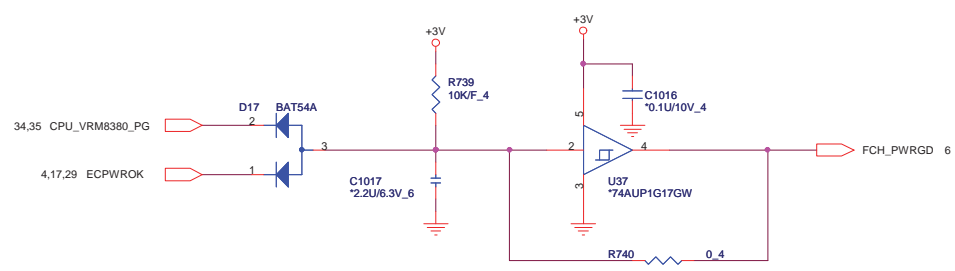
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI\_AD[27:23]



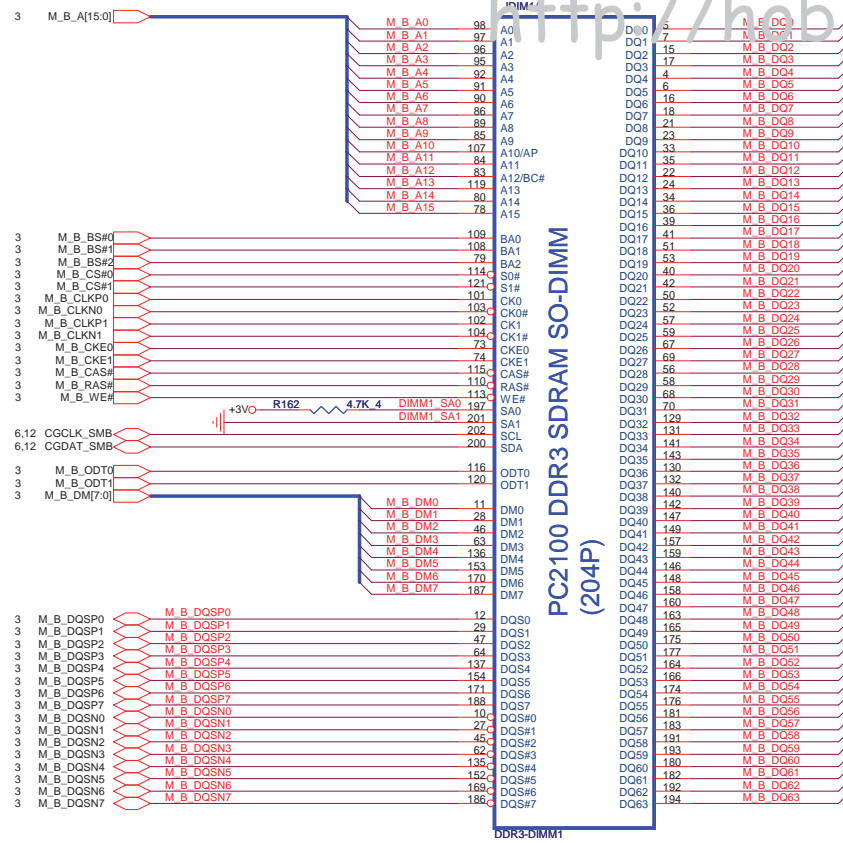
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH\_PWRGD



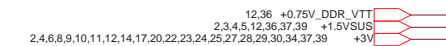
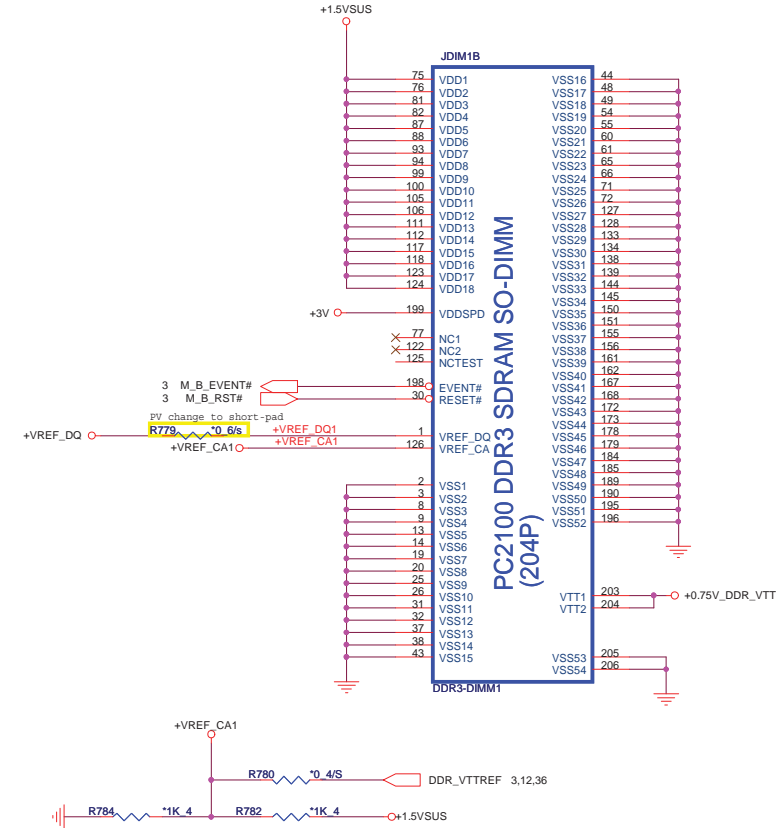
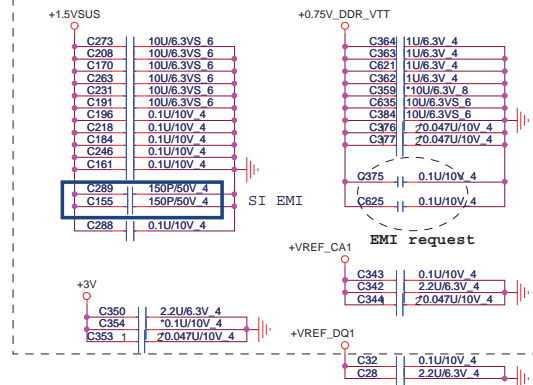






H5.2mm

Place these Caps near So-Dimm1.



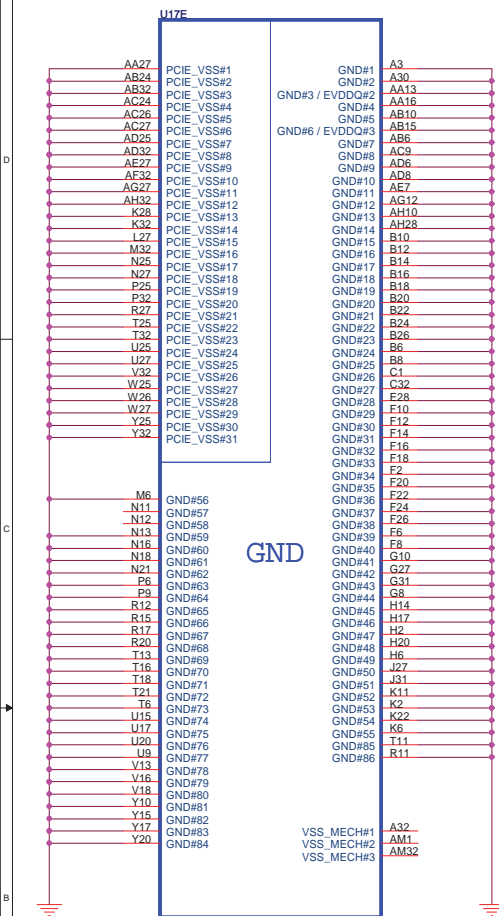
**PROJECT : R23**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A
Date: Tuesday, May 03, 2011	Sheet 13 of 40	



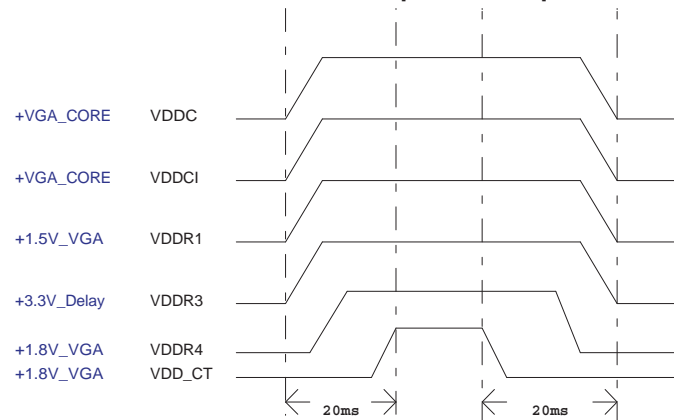




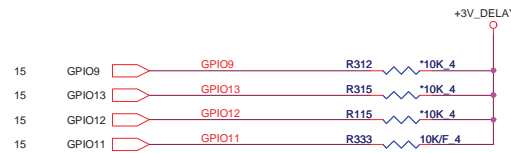


Seymour-S3  
AJ080900T01  
FCBGA631-AMD-M92-S2

### Power Up/Down Sequence



Seymour-S3  
AJ080900T01  
FCBGA631-AMD-M92-S2



### Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

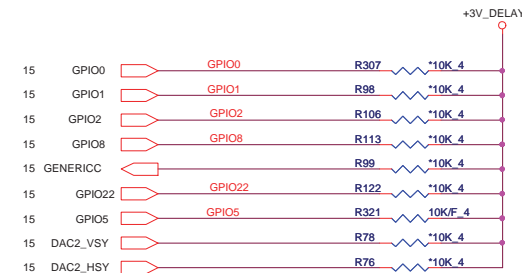
### AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21\_BB\_EN

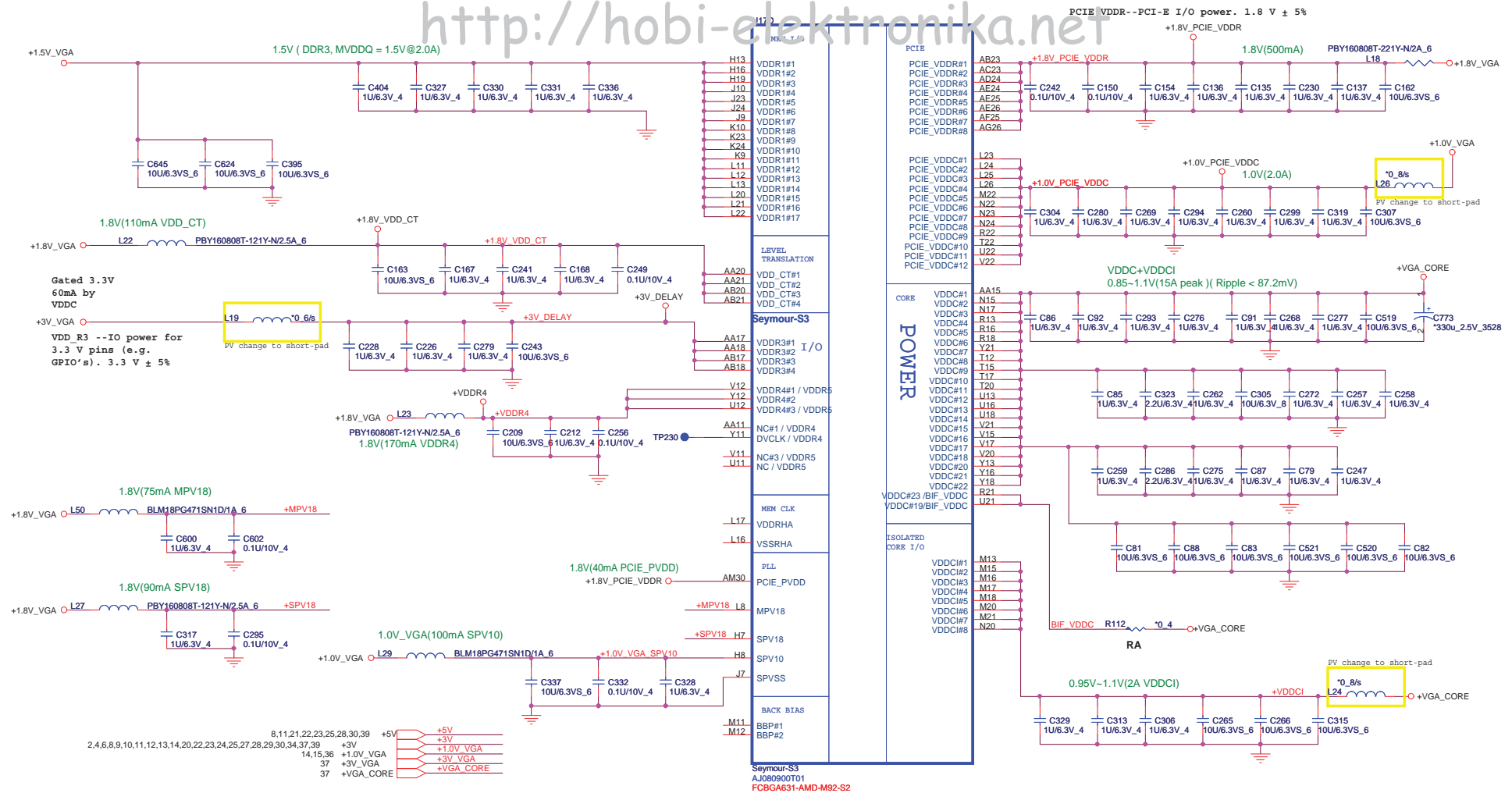


15,17 +3V\_DELAY

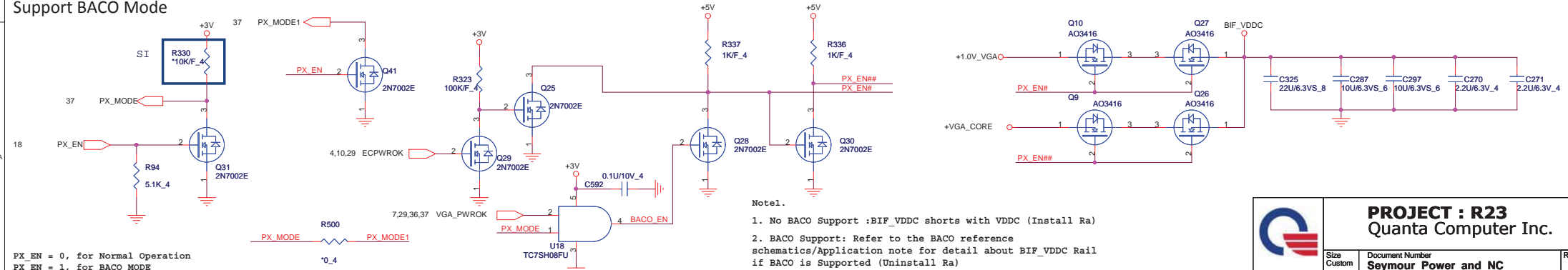


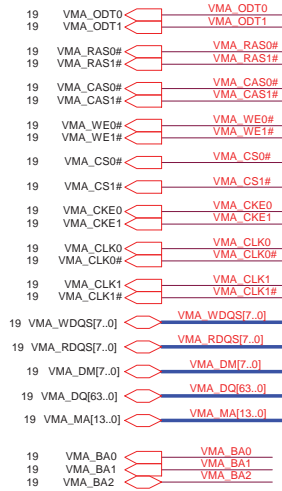
**PROJECT : R23**  
Quanta Computer Inc.

Size Custom Document Number Seymour GND / LVDS/ Straps Rev 1A  
Date: Tuesday, May 03, 2011 Sheet 16 of 40



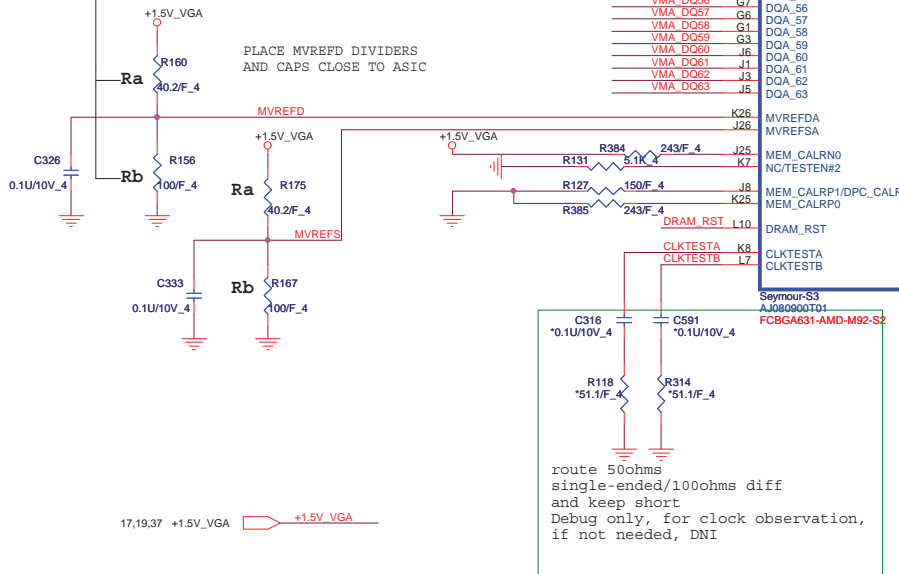
Support BACO Mode
-------------------



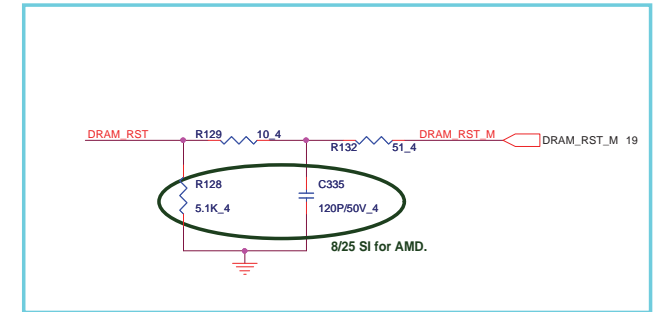
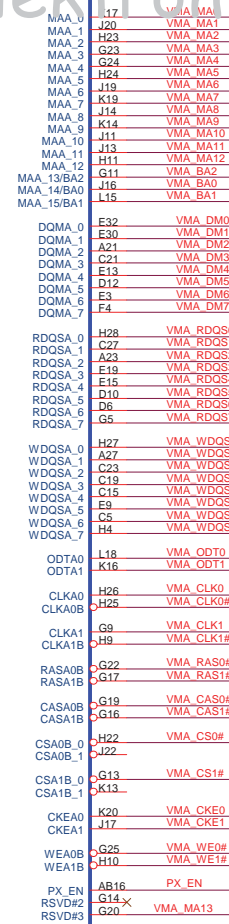


support 1Gbit  
VRAM ( 64M X 16 )

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



### MEMORY INTERFACE




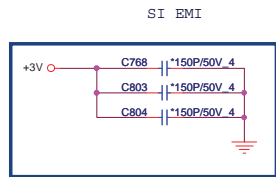
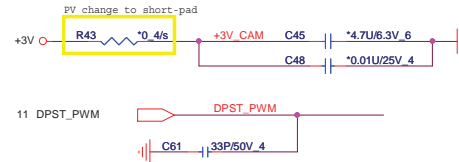
**PROJECT : R23**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour/MEM_Interface	1A
Date: Tuesday, May 03, 2011	Sheet 18 of 40	





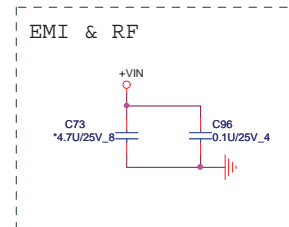
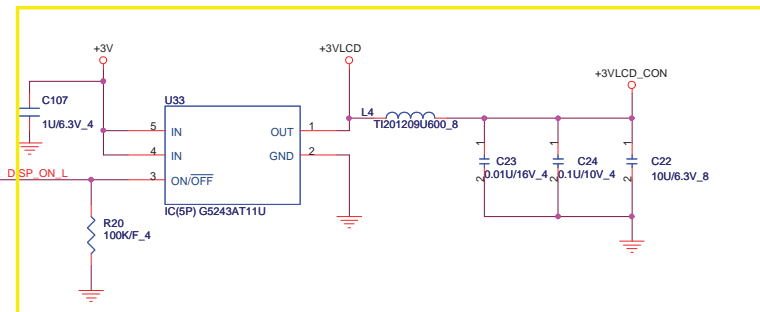
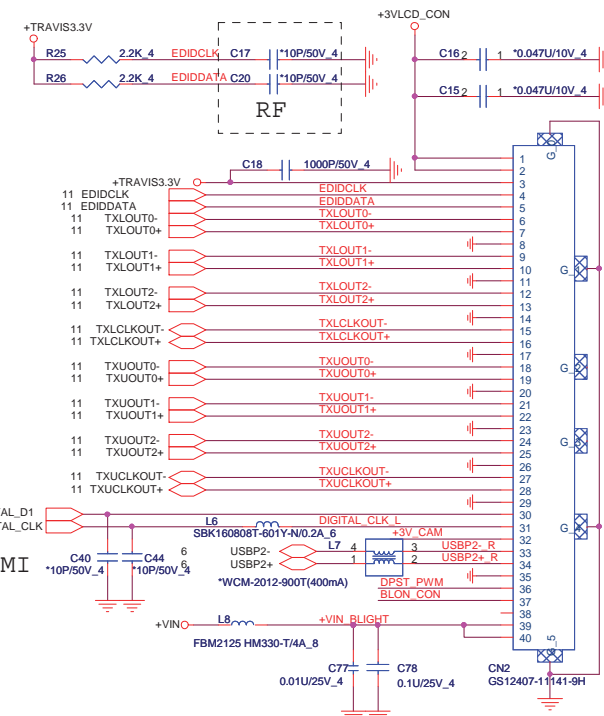
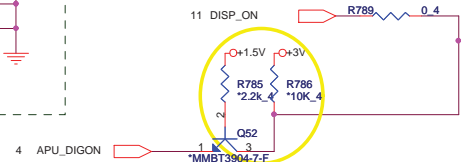
	<b>PROJECT : R23</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>Seymour VRAM(DDR3 BGA96)</b>	Rev 3A
	Date: Tuesday, May 02 2014	Sheet 40 of 40	



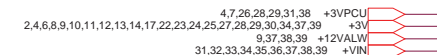
follow L7 Location

USBP2+ R44 0.4/4 USBP2+ R

USBP2+ R46 0.4/4 USBP2+ R

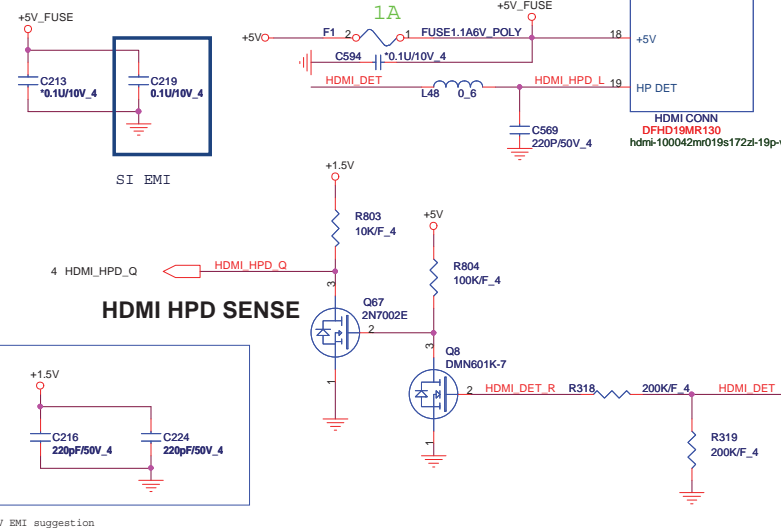
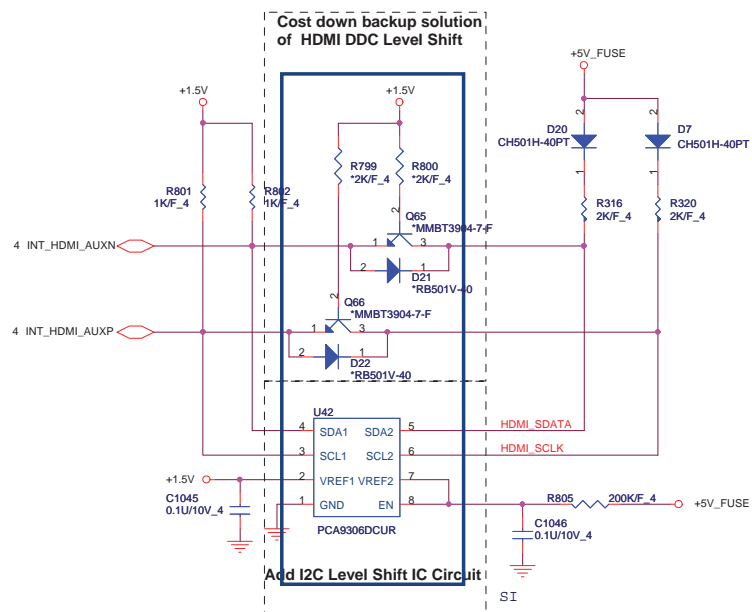
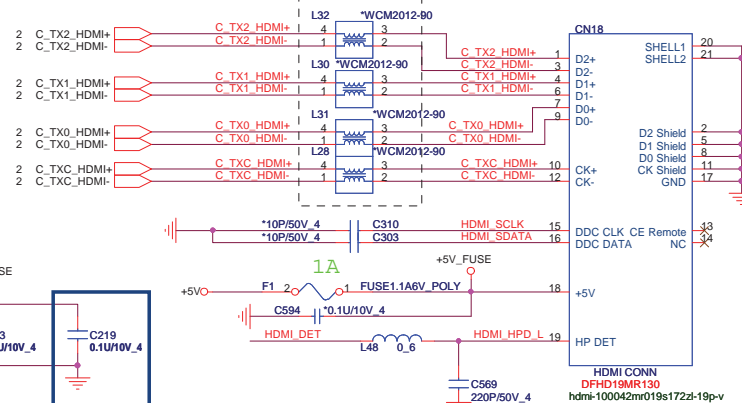
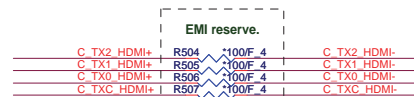
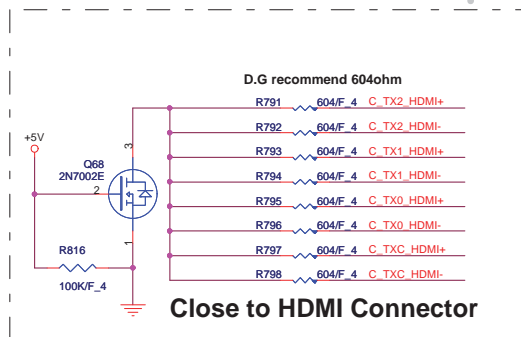
[illegible]

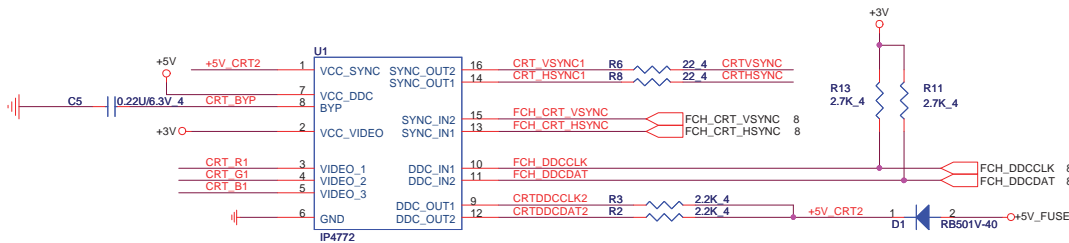
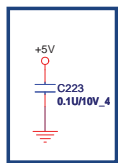
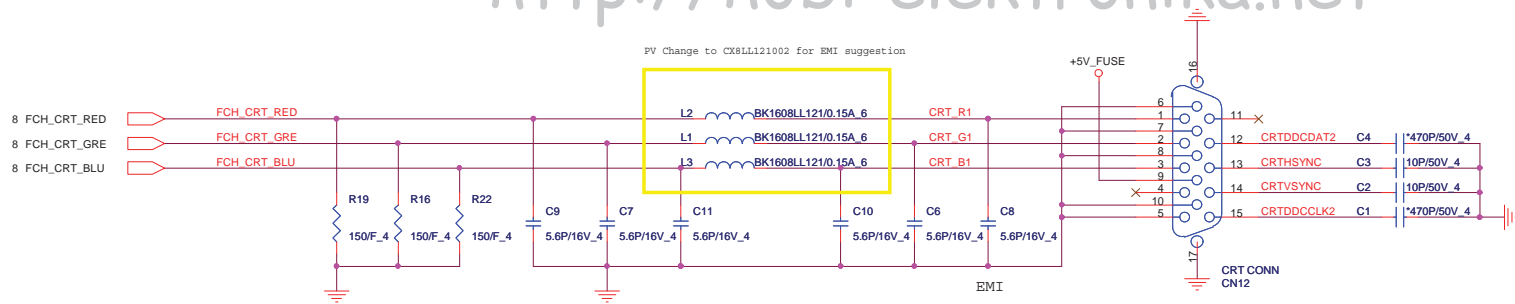
PV change for reduce circuit:



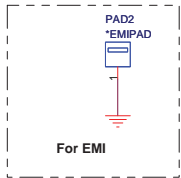
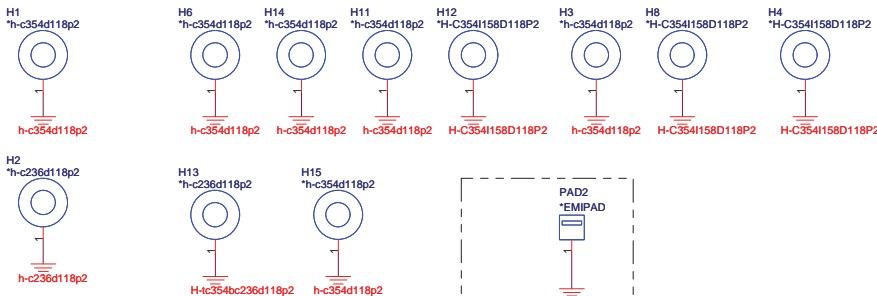
**PROJECT : R23**  
Quanta Computer Inc.

Size Custom	Document Number <b>LCD CONN/LID/CAM</b>	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 20 of 40

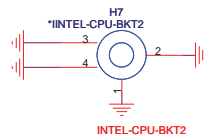




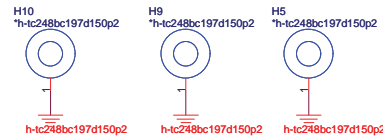
HOLE




CPU

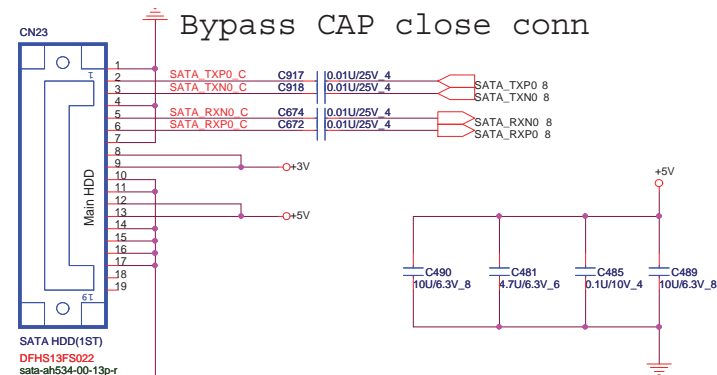


VGA

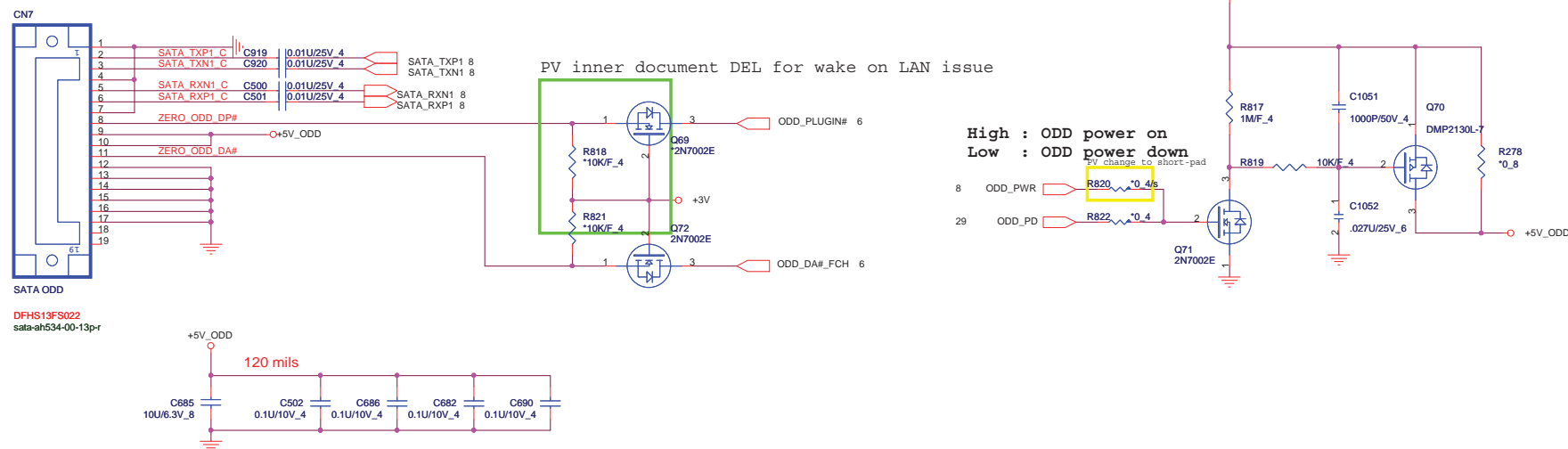


			<b>PROJECT : R23</b> Quanta Computer Inc.		Rev 1A
Size Custom	Document Number <b>CRT,Hole</b>		Date: Tuesday, May 03, 2011		
		Sheet	22	of	40

## SATA HDD CONNECTOR



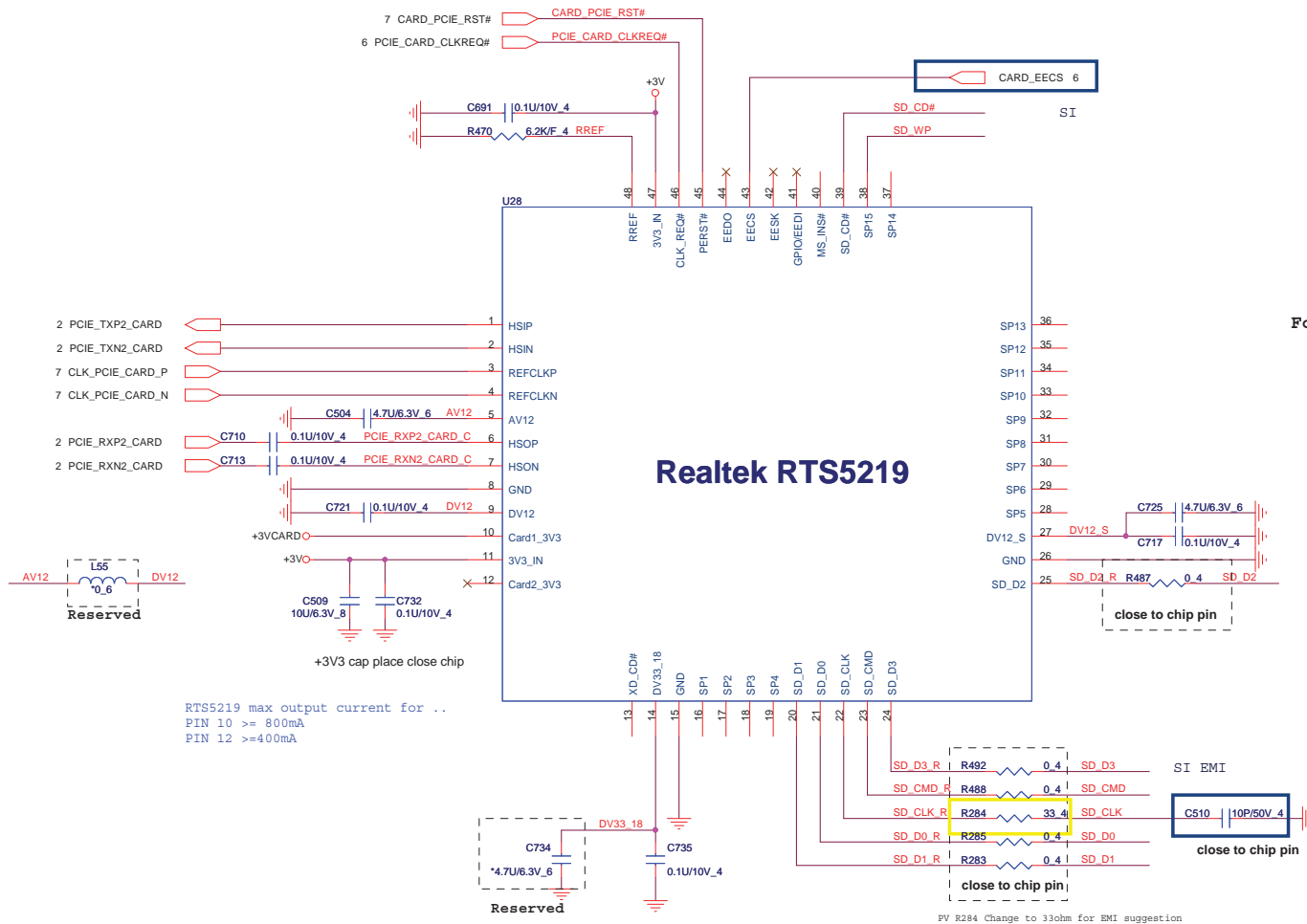
**SATA ODD CONNECTOR** SATA ODD



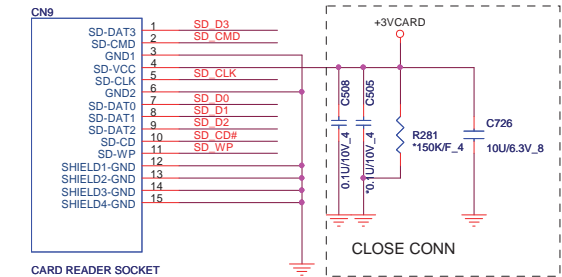
**PROJECT : R23**  
Quanta Computer Inc.

Size Custom	Document Number <b>HDD/ODD/FAN</b>	Rev 1A
Date: Wednesday, May 04, 2011		Sheet 23 of 40



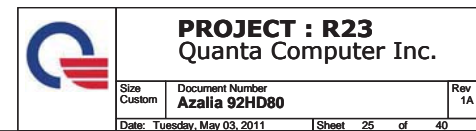


Footprint lqfp48-9x9-5-1\_6h

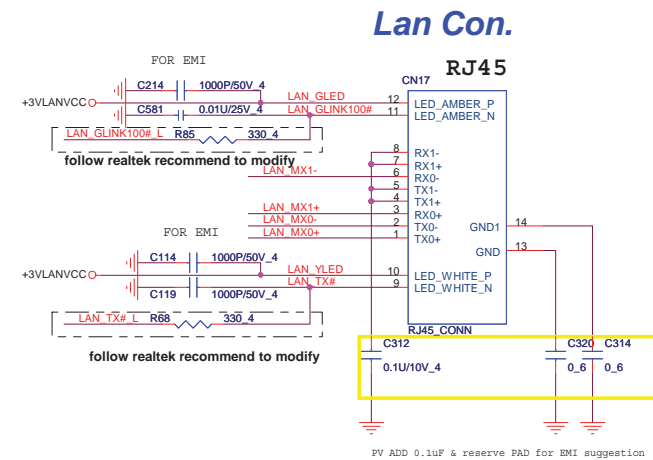
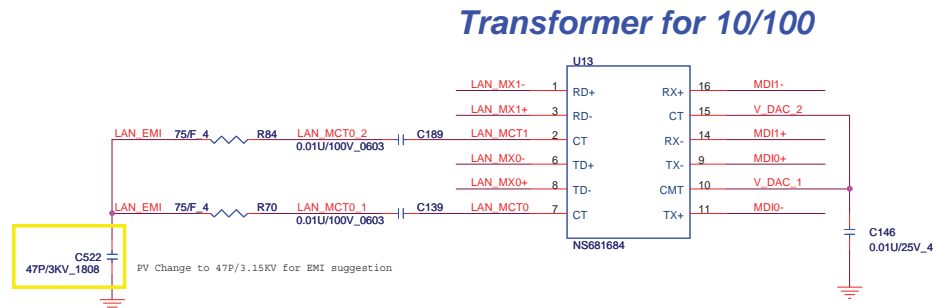
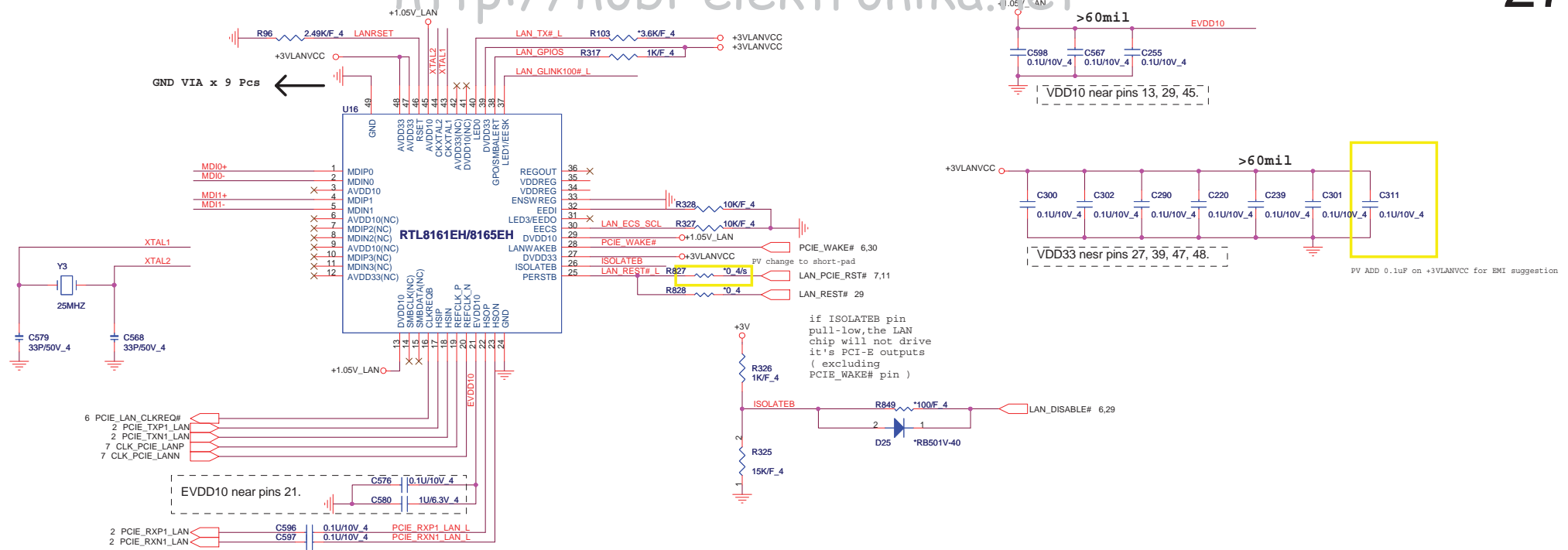


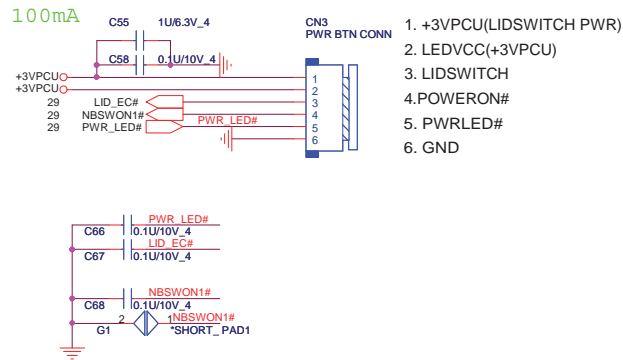
RTS5219 max output current for ..  
 PIN 10 >= 800mA  
 PIN 12 >=400mA

PV R284 Change to 33ohm for EMI suggestion

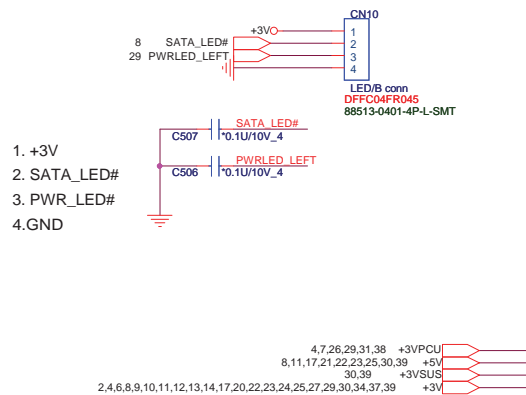




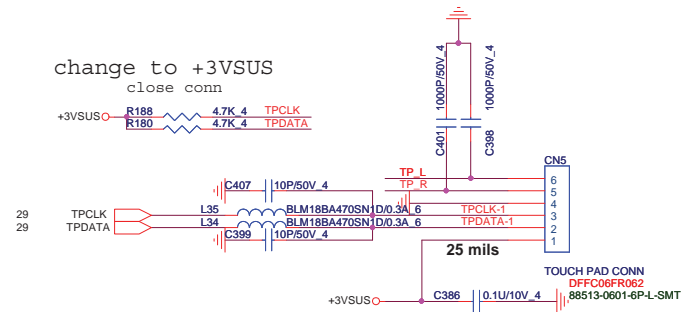




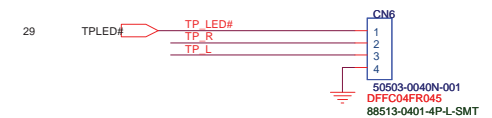
**LED Con.**



## TOUCH PAD Con.

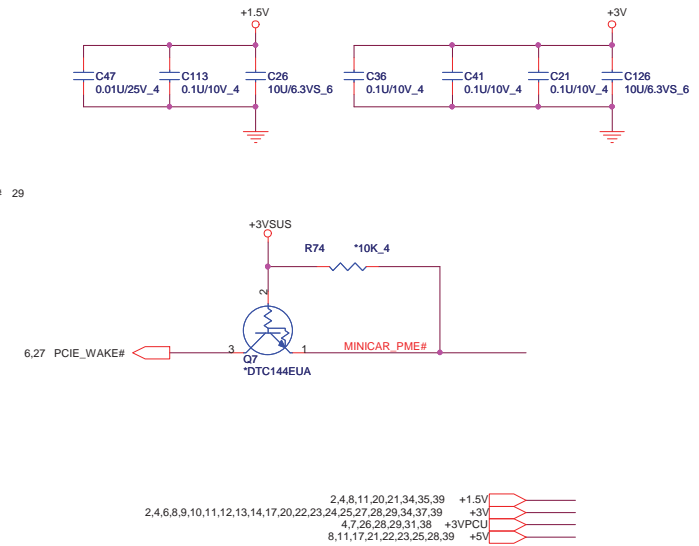


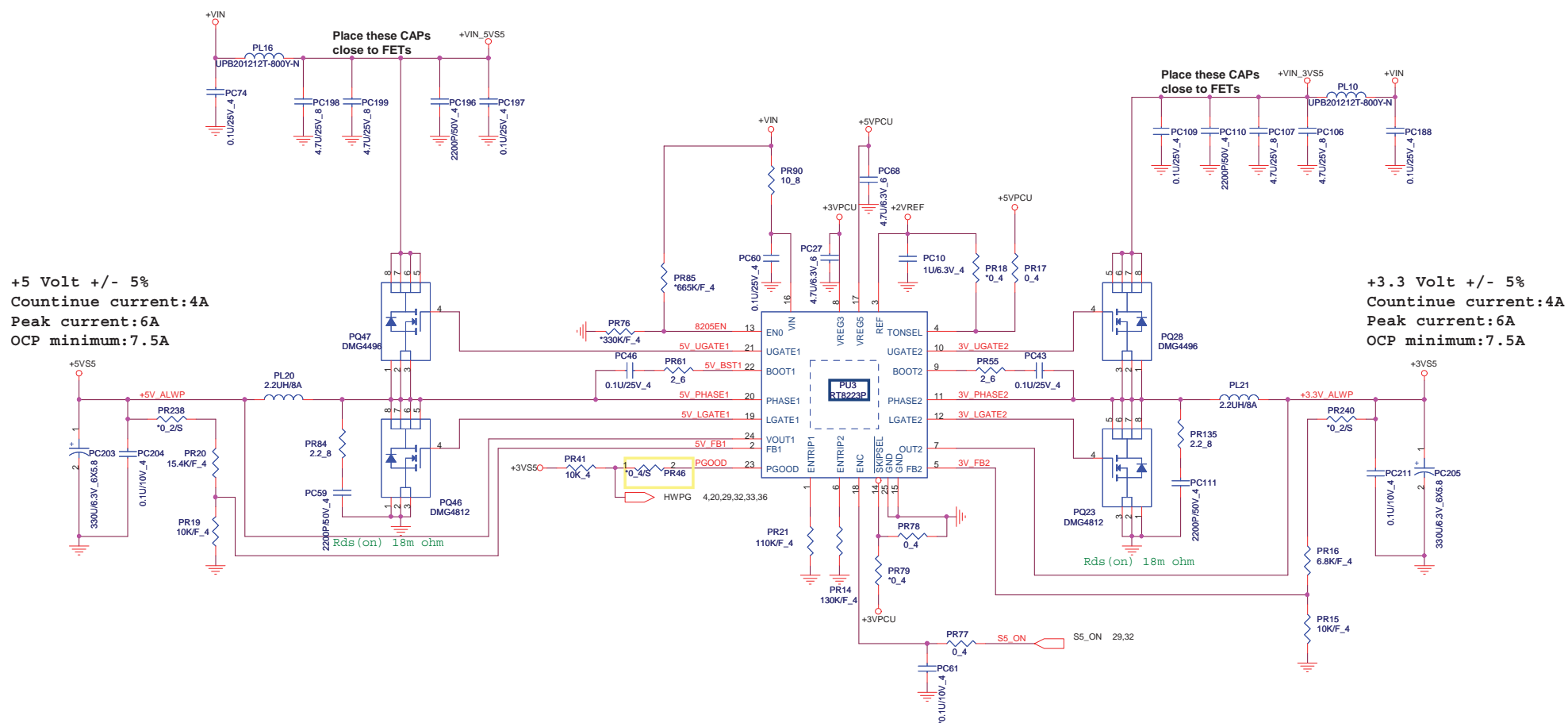
**To TOUCH PAD SW board**

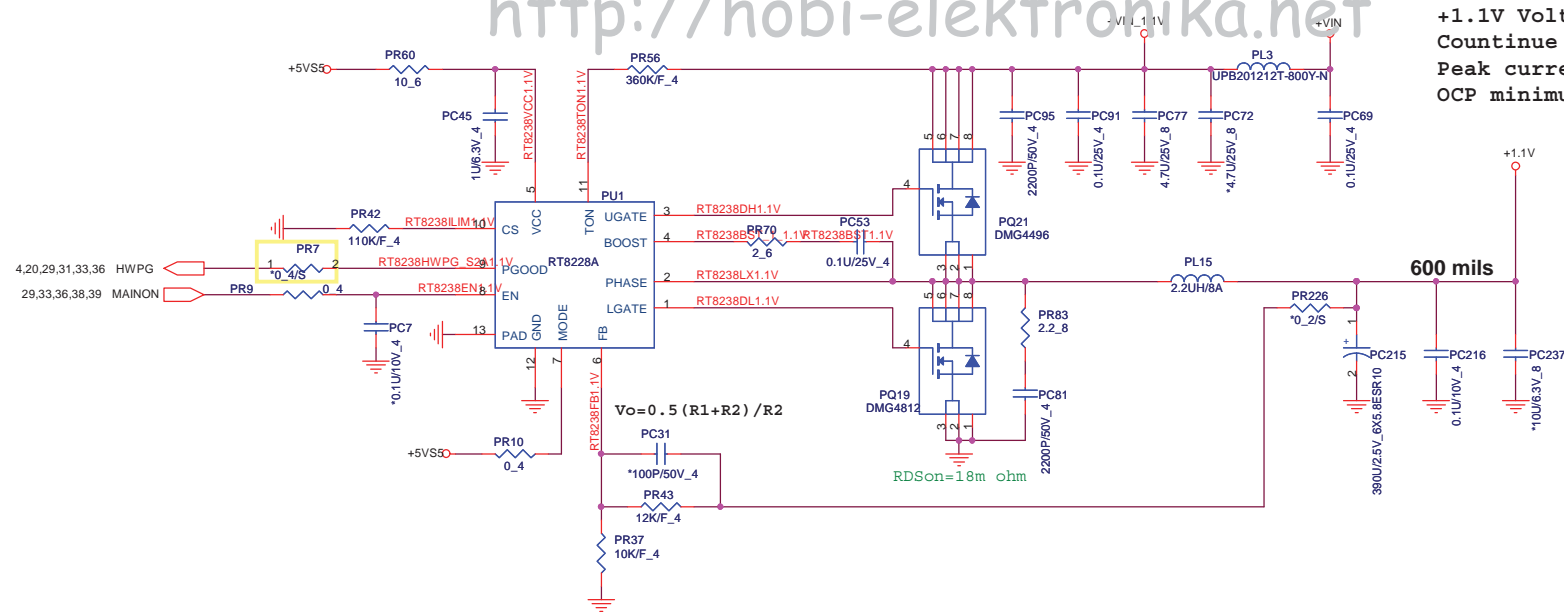




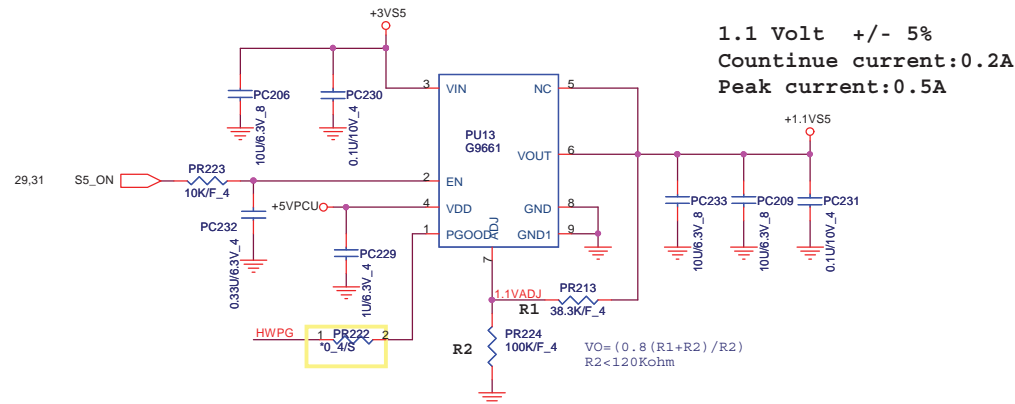


**WLAN**





+1.1V Volt +/- 5%  
 Countinue current:3A  
 Peak current: 4A  
 OCP minimum:6A

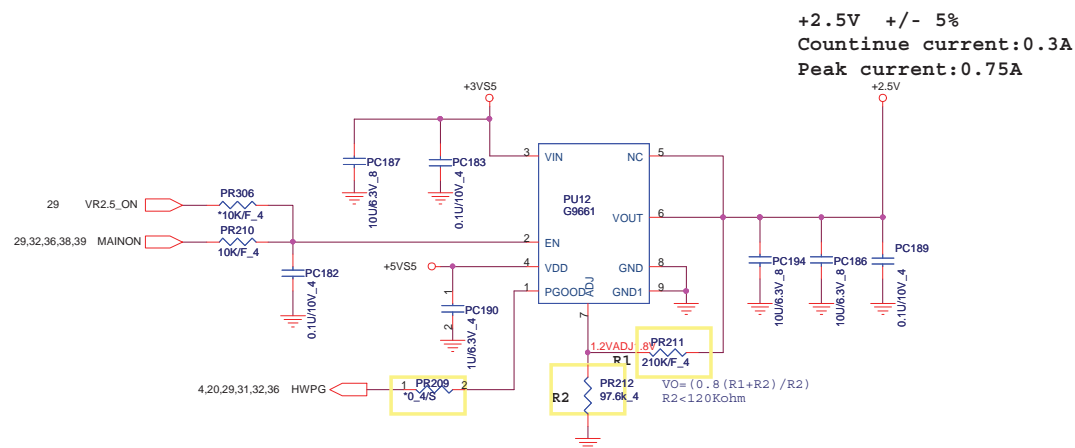
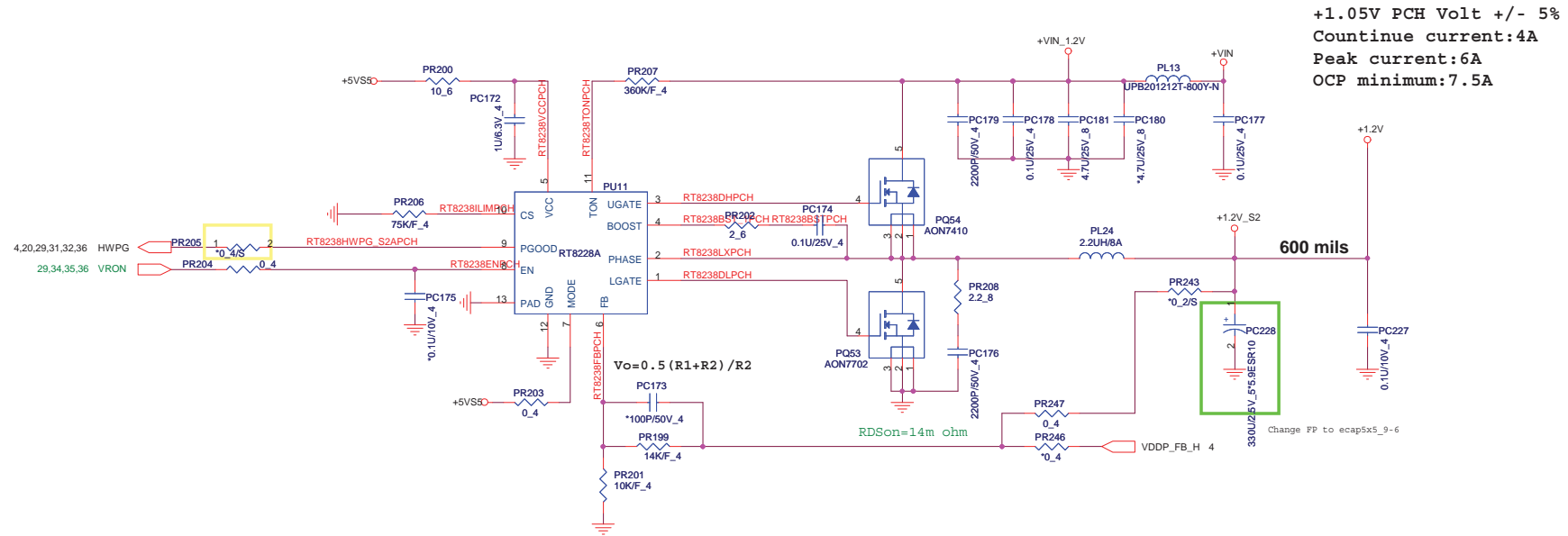


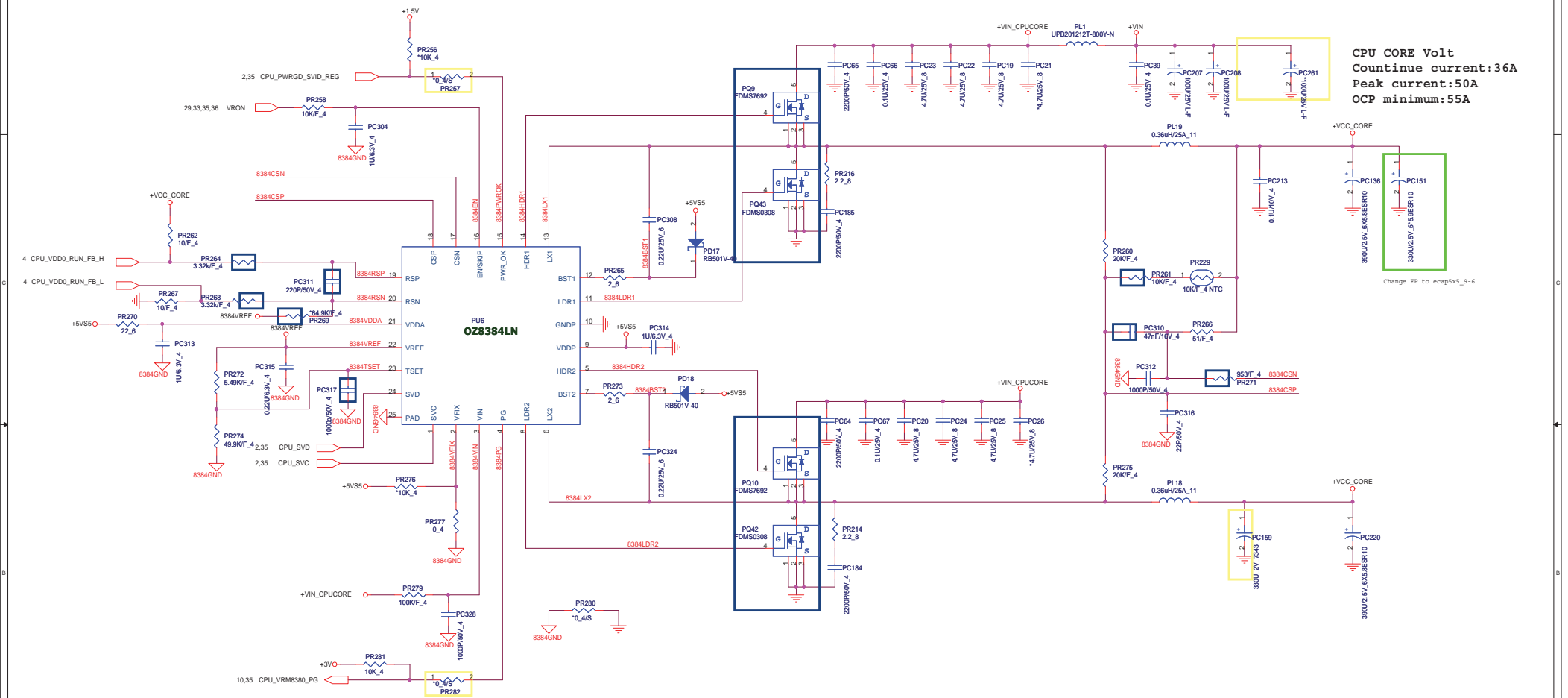
1.1 Volt +/- 5%  
 Countinue current:0.2A  
 Peak current:0.5A



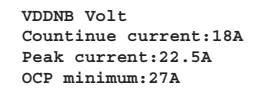
**PROJECT : R23**  
 Quanta Computer Inc.

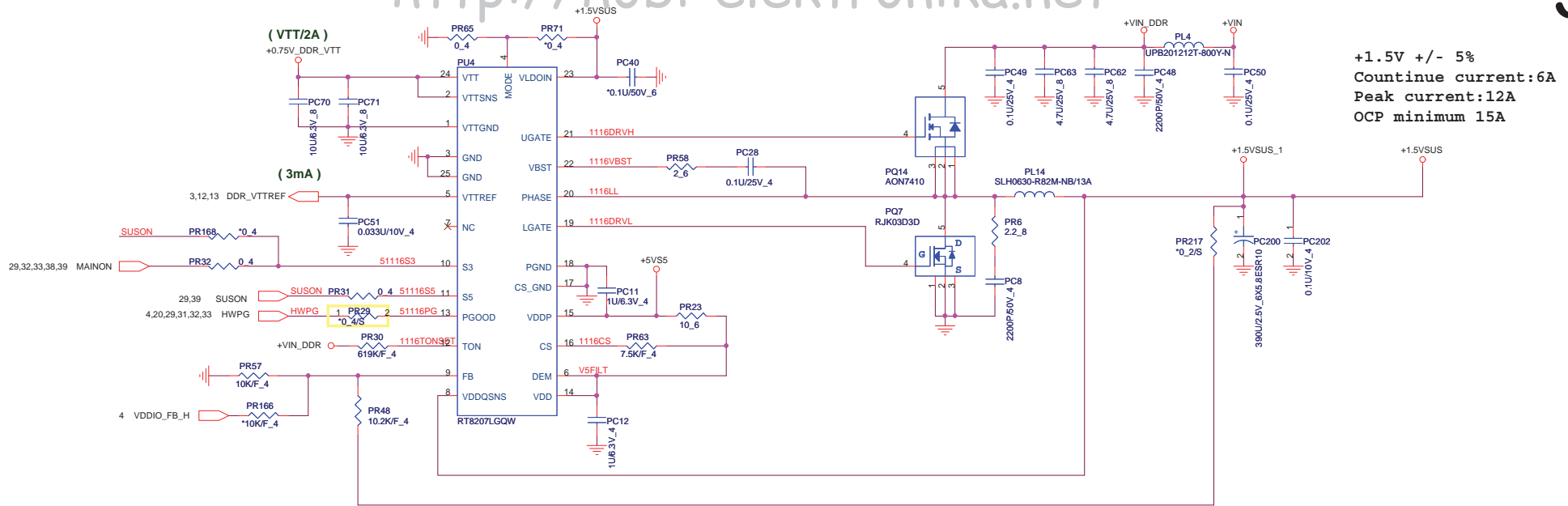
Size Custom	Document Number <b>VGA Core/+1.8VGF/+1.0VGF</b>	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 32 of 40



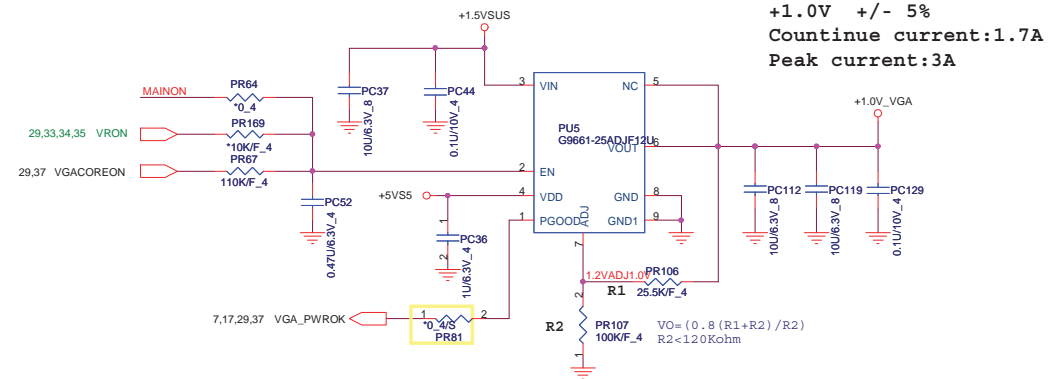
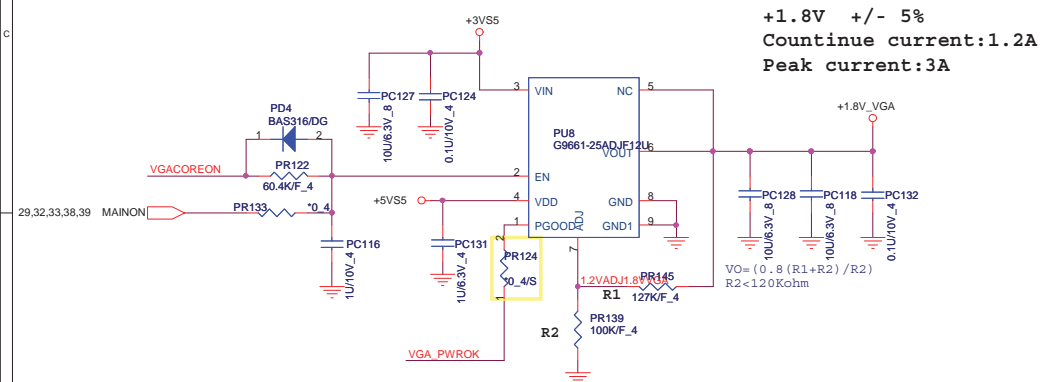









SG & Discrete Only



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$$V_o = 0.75 (R_1 + R_2) / R_2$$